

In the Claims:

With claims 1-18 and 20-24 pending, please cancel claims 14-18 and 20-23 as indicated in the list of pending claims to follow.

1. (Previously Presented) An apparatus comprising:

a variable delay isolation buffer having a signal input, a signal output, and a variable delay control input for selectively varying a delay caused by the variable delay isolation buffer in a signal traveling from the signal input to the signal output; and

a delay control circuit having an output providing the variable delay control input of the variable delay isolation buffer, the delay control circuit setting a delay control voltage potential at its output to control delay through the variable delay isolation buffer to substantially match delay through a time delay reference.

2. (Previously Presented) An apparatus comprising:

a variable delay isolation buffer having a signal input, a variable delay control input, and an output; and

a delay control circuit having an output providing the variable delay control input of the variable delay isolation buffer, the delay control circuit setting a delay control voltage potential at its output to control delay through the variable delay isolation buffer to substantially match delay through a time delay reference, wherein the delay control circuit comprises:

a reference delay line;

a reference buffer having a signal input, a variable delay control input, and an output; and

a phase comparator having a first input connected to reference delay line, a second input connected to the output of the reference buffer, and having an output connected to the variable delay control inputs of the reference buffer and the variable delay isolation buffer.

3. (Original) The apparatus of claim 2, wherein the variable delay isolation buffer and the reference buffer are fabricated on a single wafer.

4. (Original) The apparatus of claim 1, further comprising:

driver buffers each having a signal input connected to the output of the variable delay isolation buffer, and a power supply input connected to receive a system voltage.

5. (Original) The apparatus of claim 4, wherein each of the driver buffers and the variable delay isolation buffer comprises a CMOS inverter.

6 (Original) The apparatus of claim 1, wherein the variable delay isolation buffer comprises a differential amplifier with a variable current sink providing the variable delay control input.

7. (Original) The apparatus of claim 2 further comprising:

an oscillator connected by the reference delay line to the first input of the phase comparator and by the reference buffer to the second input of the phase comparator; and  
a loop filter connecting the output of the phase comparator to the variable delay control inputs of the reference buffer and the variable delay isolation buffer.

8. (Original) The apparatus of claim 7,

wherein the variable delay control inputs of the reference buffer and isolation buffer each comprise a high level voltage input line and a low level voltage input line,

wherein a system voltage comprises a system high voltage and a system low voltage power supply, and

wherein the loop filter connects the phase comparator output to the high and low level voltage input lines of the reference buffer and the variable delay isolation buffer, the loop filter comprising a means for integrating and centerlining the phase comparator output to provide an integrated signal on the high level voltage line relative to the high voltage power supply and an integrated signal on the low level voltage line relative to the low voltage power supply, so that the integrated signals on the high and low level voltage lines are centered between the high and low level voltage power supplies.

9. (Original) The apparatus of claim 8, wherein the means for integrating and centerlining comprises:

first resistor having a first terminal connected to the output of the phase comparator, and a second terminal;

a second resistor having a first terminal connected to a system high voltage power supply line to receive the system high voltage power supply, and having a second terminal;

a first capacitor;

a first amplifier having a noninverting (+) input connected to the second terminal of the first and second resistors, an inverting (-) input, and having an output connected to the high voltage input lines of the reference buffer and the variable delay isolation buffer, wherein the output of the first amplifier is fed back to its inverting (-) input through the first capacitor;

a third resistor having a first terminal connected to the output of the phase comparator, and a second terminal;

a fourth resistor having a first terminal connected to a system low voltage power supply line to receive a system low voltage potential, and having a second terminal;

a second capacitor; and

a second amplifier having an inverting (-) input connected to the second terminal of the third resistor, a non-inverting (+) input connected to the second terminal of the fourth resistor, and having an output connected to the low voltage input lines of the reference buffer and the variable delay isolation buffer, wherein the output of the second amplifier is fed back to its inverting (-) input through the second capacitor.

10. (Original) The apparatus of claim 2, wherein the variable delay isolation buffer comprises:

a first inverter having a variable delay control input receiving the control voltage potential as varied from a system voltage; and

a second inverter connected in series with the first inverter, the second inverter having a power supply input connected to the receive the system voltage, and

wherein the reference buffer comprises:

a first inverter having a variable delay control input receiving the control voltage potential as varied from a system voltage; and

a second inverter connected in series with the first inverter, the second inverter having a power supply input connected to the receive the system voltage.

11. (Original) The apparatus of claim 4,

wherein the signal input of the variable delay isolation buffer forms a first terminal of a channel on a probe card with the second terminal of the channel configured for connection to a tester for transmitting and receiving test signals for testing devices on a wafer, and

wherein the output of each of the driver buffers is configured to connect to a respective probe for contacting devices on the wafer.

12. (Original) An apparatus of claim 1, wherein the variable delay isolation buffer comprises a first variable delay isolation buffer, the apparatus further comprising:

additional variable delay isolation buffers each having a signal input connected in common with the first variable delay isolation buffer, a variable delay control input connected to the output of the delay control circuit, and having an output.

13. (Original) The apparatus of claim 12 further comprising:

driver buffers each having a signal input connected to the output of one of the first and additional variable delay isolation buffers and having a power supply input connected to receive a system voltage.

14-23. (Cancelled)

24. (New) The apparatus of claim 1, wherein the variable delay isolation buffer and the delay control circuit are provided on a probe card, wherein the output of each variable delay isolation buffer is connected to a separate probe on the probe card.